

P-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	- 40
$R_{DS(on)}$ (Ω) at $V_{GS} = -10$ V	0.006
$R_{DS(on)}$ (Ω) at $V_{GS} = -4.5$ V	0.007
I_D (A)	-80
Configuration	Single

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- SGT technology Power MOSFET
- Package with Low Thermal Resistance
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

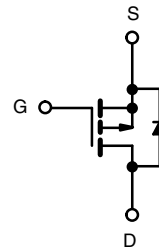


RoHS
COMPLIANT
HALOGEN
FREE

TO-263



Top View



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	- 40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 125^\circ\text{C}$	
Continuous Source Current (Diode Conduction) ^a	I_S	-70	
Pulsed Drain Current ^b	I_{DM}	-240	
Single Pulse Avalanche Current	I_{AS}	-70	
Single Pulse Avalanche Energy	E_{AS}	1345	mJ
Maximum Power Dissipation ^b	P_D	$T_C = 25^\circ\text{C}$	W
		$T_C = 125^\circ\text{C}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	50	$^\circ\text{C}/\text{W}$
Junction-to-Case (Drain)	R_{thJC}	0.6	

Notes

- Package limited.
- Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.

SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA		- 40	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA		- 1.0	-	-3.0	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = - 40 V	-	-	- 1	μA
		V _{GS} = 0 V	V _{DS} = - 40 V, T _J = 125 °C	-	-	- 50	
		V _{GS} = 0 V	V _{DS} = - 40 V, T _J = 150°C	-	-	- 250	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = - 10 V	V _{DS} ≤ - 5 V	- 30	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 20 A	-	0.006	-	Ω
		V _{GS} = - 10 V	I _D = - 20 A, T _J = 125 °C	-	0.009	-	
		V _{GS} = - 10 V	I _D = - 20 A, T _J = 150 °C	-	0.015	-	
		V _{GS} = - 4.5 V	I _D = -20 A	-	0.008	-	
Forward Transconductance ^b	g _{fs}	V _{DS} = - 15 V, I _D = -20 A		-	35	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = - 25 V, f = 1 MHz	-	8000	-	pF
Output Capacitance	C _{oss}			-	301	-	
Reverse Transfer Capacitance	C _{rss}			-	208	-	
Total Gate Charge ^c	Q _g	V _{GS} = - 10 V	V _{DS} = - 50V, I _D = - 9.2 A	-	96	144	nC
Gate-Source Charge ^c	Q _{gs}			-	8.4	-	
Gate-Drain Charge ^c	Q _{gd}			-	23.5	-	
Gate Resistance	R _g	f = 1 MHz		1.5	3.13	4.7	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = - 50 V, R _L = 6.49 Ω I _D ≅ - 7.7 A, V _{GEN} = - 10 V, R _g = 1.0 Ω		-	11	17	ns
Rise Time ^c	t _r			-	11	17	
Turn-Off Delay Time ^c	t _{d(off)}			-	78	117	
Fall Time ^c	t _f			-	15	23	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	- 240	A
Forward Voltage	V _{SD}	I _F = - 7.7 A, V _{GS} = 0 V		-	- 0.8	- 1.5	V

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.
 c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Typical Electrical and Thermal Characteristics

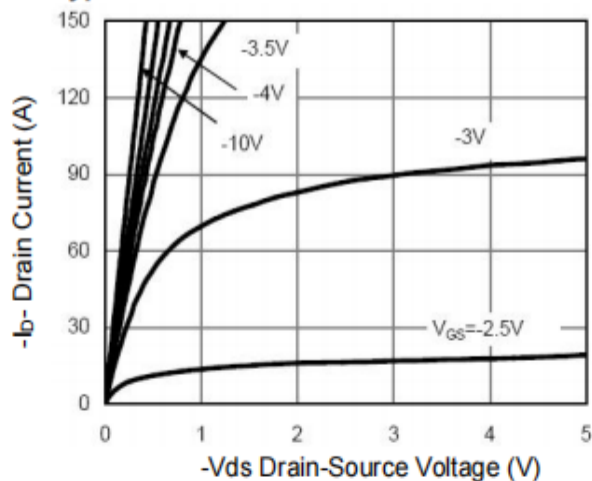


Figure 1 Output Characteristics

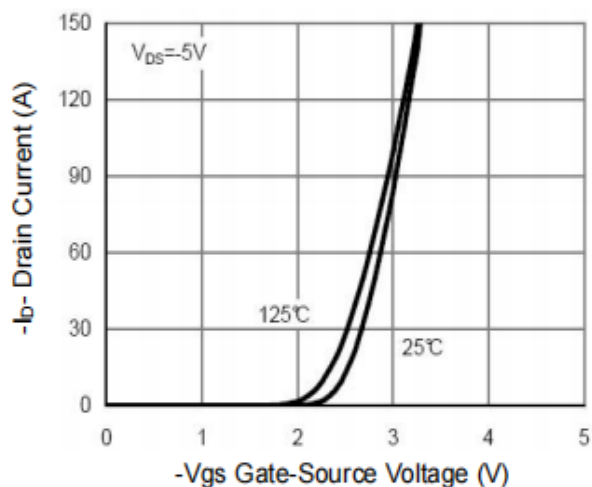


Figure 2 Transfer Characteristics

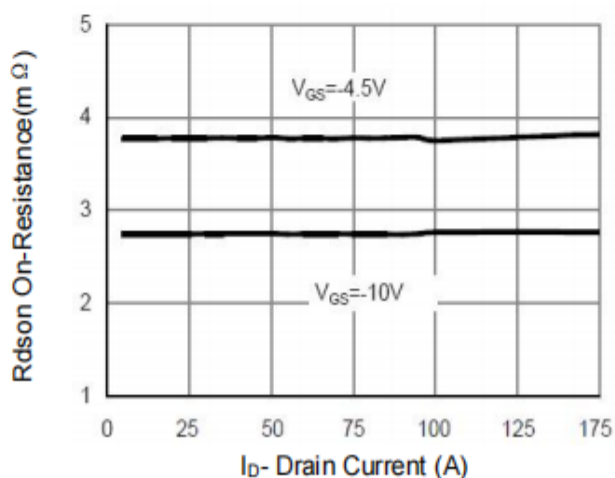


Figure 3 Rdson- Drain Current

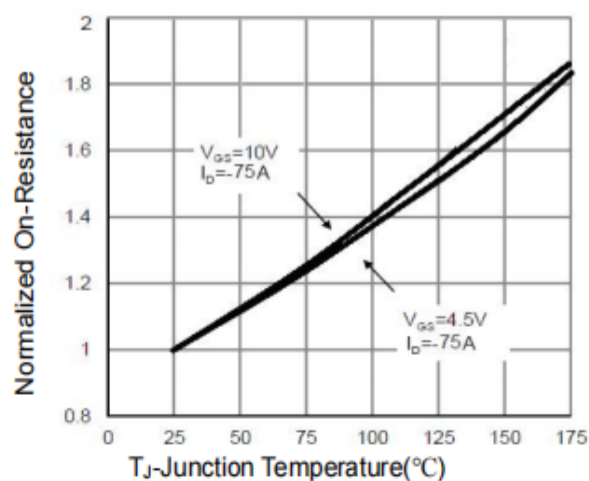


Figure 4 Rdson-Junction Temperature

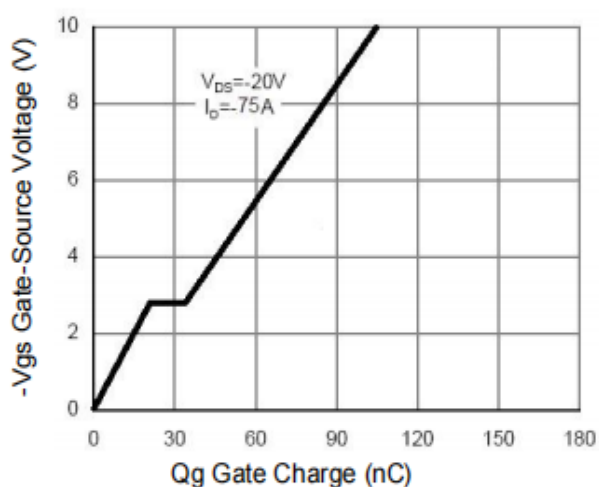


Figure 5 Gate Charge

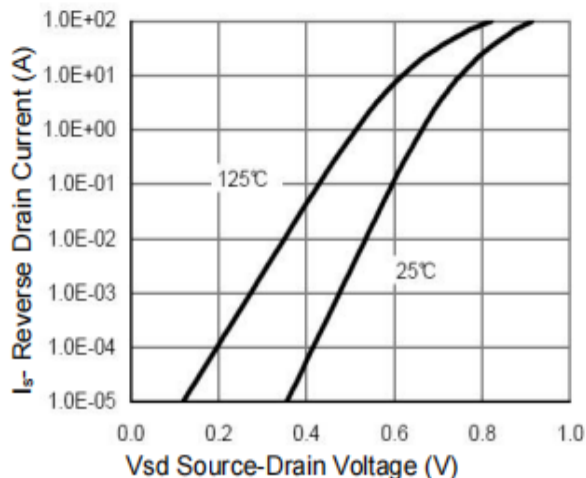


Figure 6 Source- Drain Diode Forward

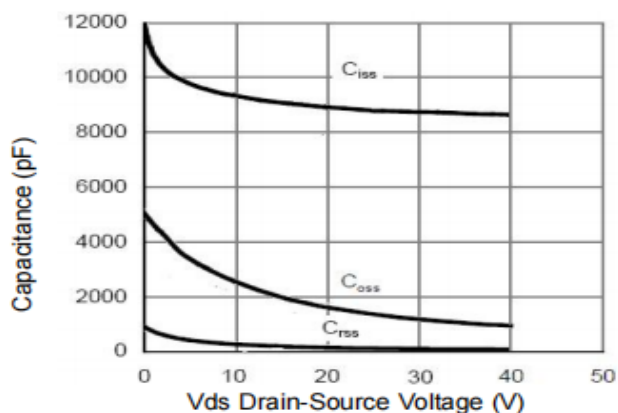


Figure 7 Capacitance vs Vds

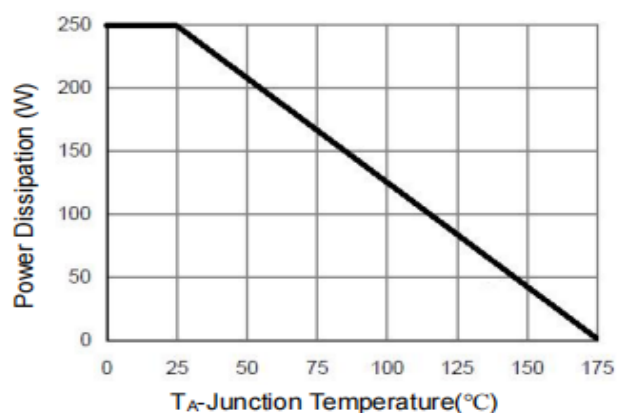


Figure 9 Power De-rating

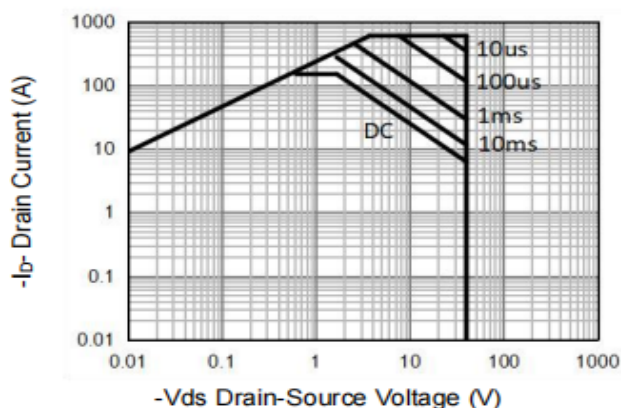


Figure 8 Safe Operation Area^(Note 3)

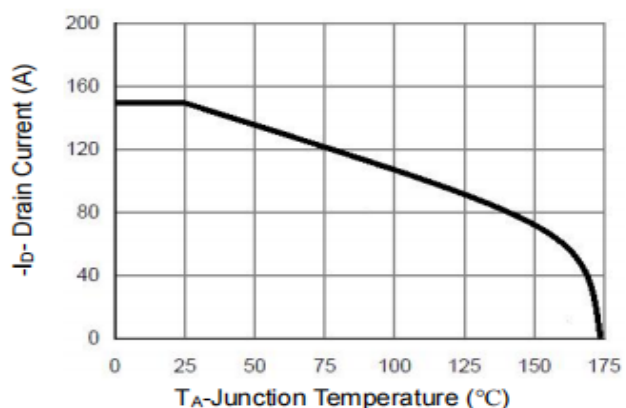


Figure 10 Current De-rating

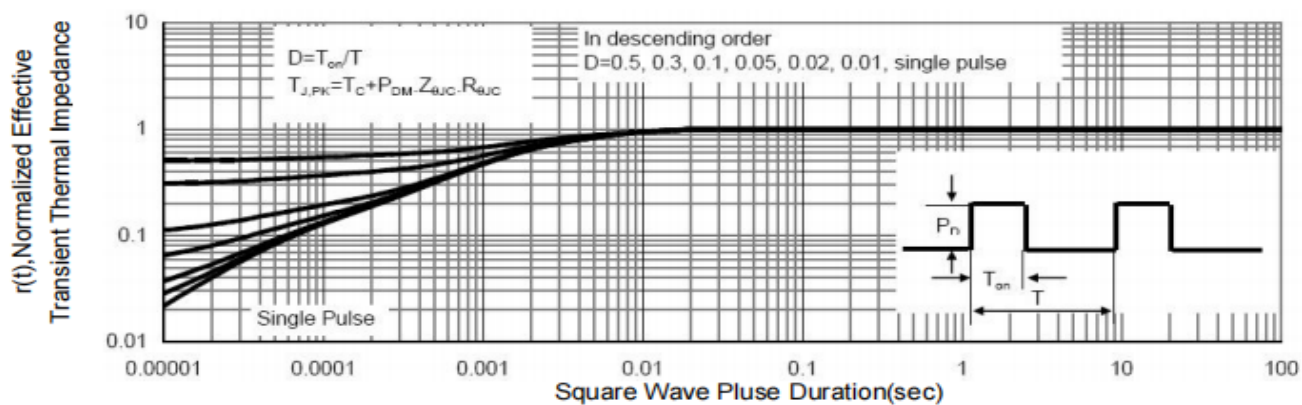
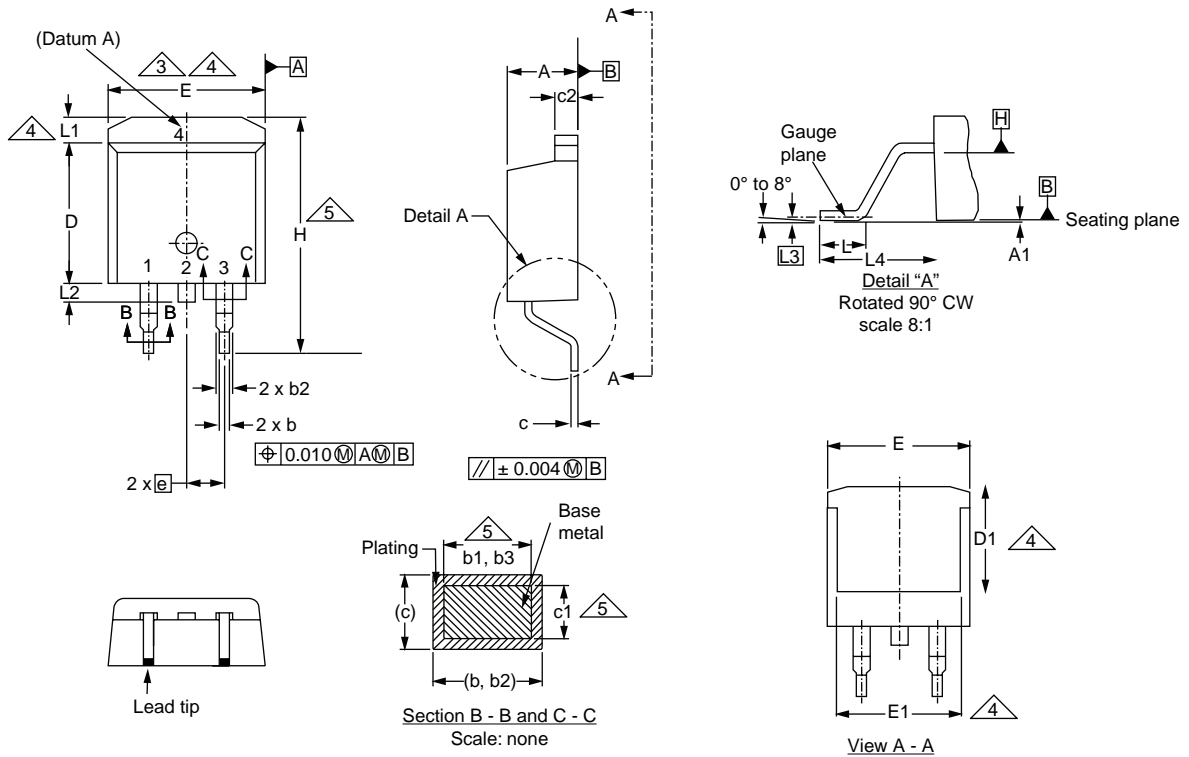


Figure 11 Normalized Maximum Transient Thermal Impedance

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	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
 DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

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