

SiHLD120-E3-VB Datasheet

N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^d	Q_g (Typ.)
100	0.080 at $V_{GS} = 10$ V	4.5	4.6 nC
	0.090 at $V_{GS} = 6$ V	4.0	

FEATURES

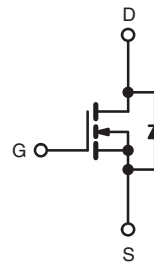
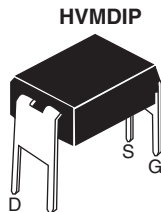
- Trench Power MOSFET
- 100 % UIS Tested

APPLICATIONS

- High Frequency Boost Converter
- LED Backlight for LCD TV



RoHS
COMPLIANT
HALOGEN
FREE



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	$T_C = 25$ °C	4.5	A
	$T_C = 70$ °C	3.5	
	$T_A = 25$ °C	2.9 ^{a, b}	
	$T_A = 70$ °C	2.3 ^{a, b}	
Pulsed Drain Current	I_{DM}	16	A
Continuous Source-Drain Diode Current	$T_C = 25$ °C	4	
	$T_A = 25$ °C	2 ^{a, b}	
Single Avalanche Current	I_{AS}	6	A
Single Avalanche Energy	E_{AS}	1.8	mJ
Maximum Power Dissipation	$T_C = 25$ °C	4.8	W
	$T_C = 70$ °C	3	
	$T_A = 25$ °C	2.4 ^{a, b}	
	$T_A = 70$ °C	1.5 ^{a, b}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}	R_{thJA}	42	53	°C/W
Maximum Junction-to-Foot (Drain)	R_{thJF}	21	26	

Notes:

- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- Maximum under steady state conditions is 85 °C/W.
- Based on $T_C = 25$ °C.

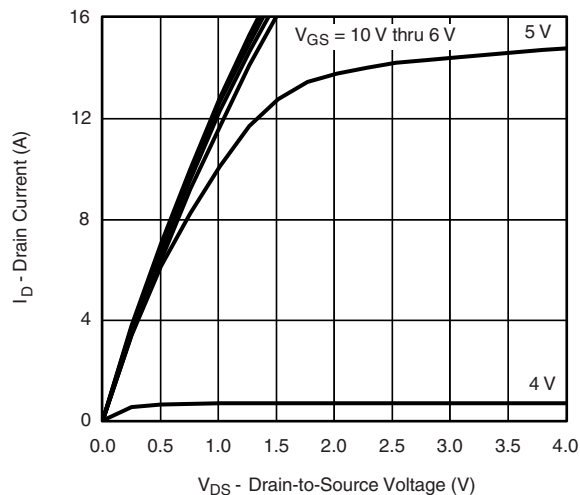
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		110		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 7.5		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	8			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 2.7 A		0.080		Ω
		V _{GS} = 6 V, I _D = 2.5 A		0.090		
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 2.7 A		7		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		370		pF
Output Capacitance	C _{oss}			40		
Reverse Transfer Capacitance	C _{rss}			20		
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 2.7 A		7.1	11	nC
		V _{DS} = 50 V, V _{GS} = 6 V, I _D = 2.7 A		4.6	7	
Gate-Source Charge	Q _{gs}			1.7		
Gate-Drain Charge	Q _{gd}			2		
Gate Resistance	R _g	f = 1 MHz		3		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 23.8 Ω I _D ≅ 2.1 A, V _{GEN} = 6 V, R _g = 1 Ω		10	15	ns
Rise Time	t _r			10	15	
Turn-Off Delay Time	t _{d(off)}			10	15	
Fall Time	t _f			10	15	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 23.8 Ω I _D ≅ 2.1 A, V _{GEN} = 10 V, R _g = 1 Ω		10	15	
Rise Time	t _r			10	15	
Turn-Off Delay Time	t _{d(off)}			12	20	
Fall Time	t _f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			4	A
Pulse Diode Forward Current	I _{SM}				8	
Body Diode Voltage	V _{SD}	I _S = 2.1 A, V _{GS} = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 2.1 A, dI/dt = 100 A/μs, T _J = 25 °C		50	80	ns
Body Diode Reverse Recovery Charge	Q _{rr}			75	120	nC
Reverse Recovery Fall Time	t _a			28		ns
Reverse Recovery Rise Time	t _b			22		

Notes:

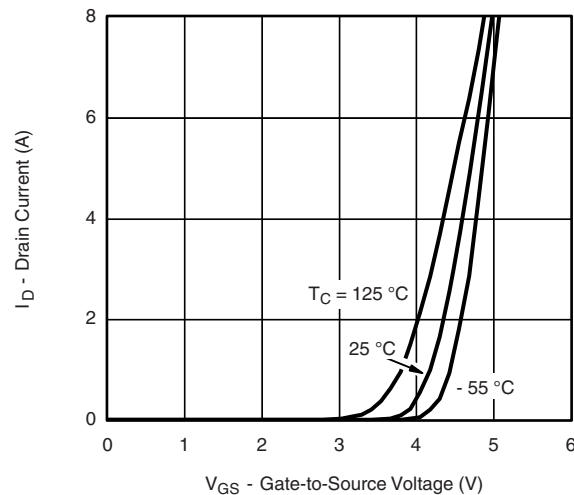
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b. Guaranteed by design, not subject to production testing.

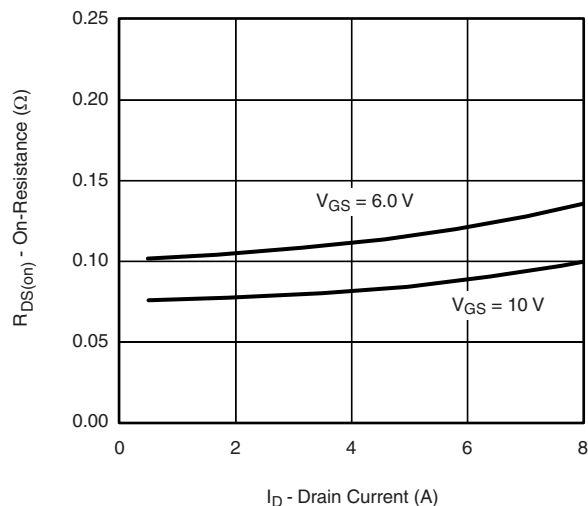
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


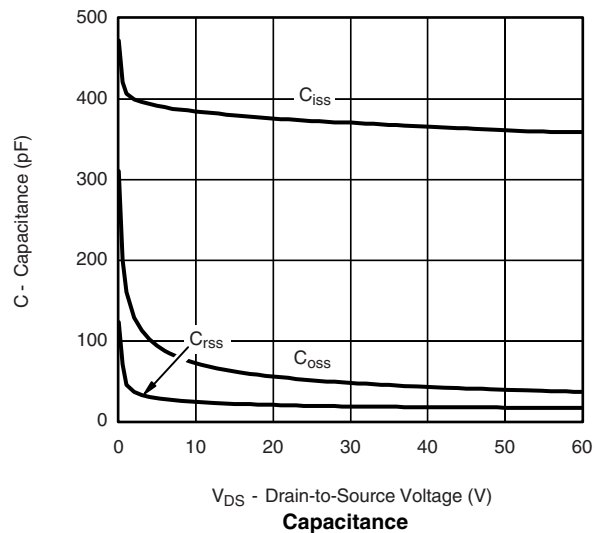
V_{DS} - Drain-to-Source Voltage (V)
Output Characteristics



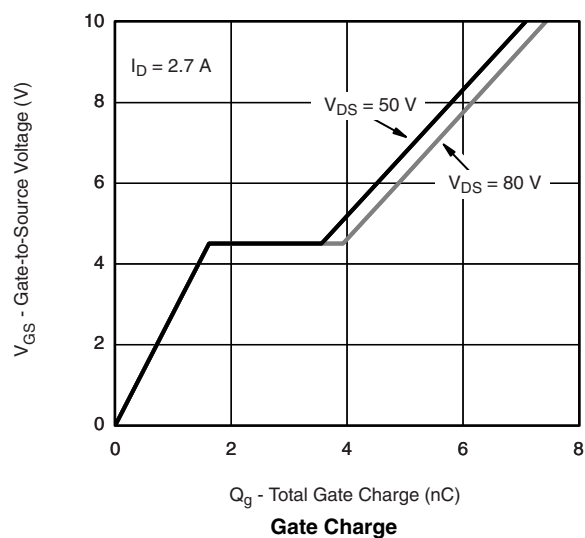
V_{GS} - Gate-to-Source Voltage (V)
Transfer Characteristics



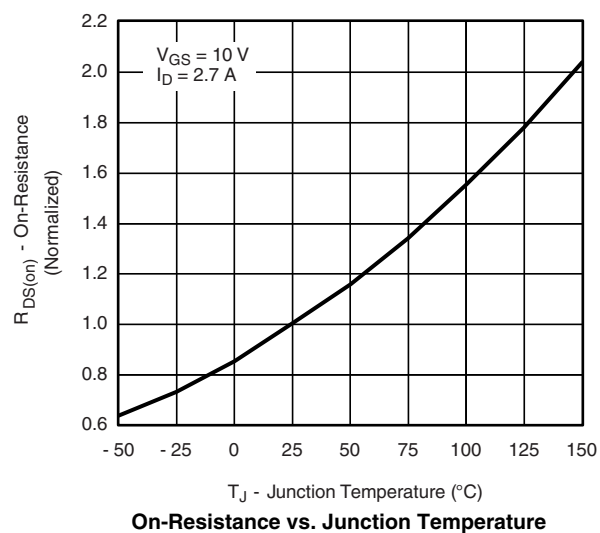
I_D - Drain Current (A)
On-Resistance vs. Drain Current



V_{DS} - Drain-to-Source Voltage (V)
Capacitance

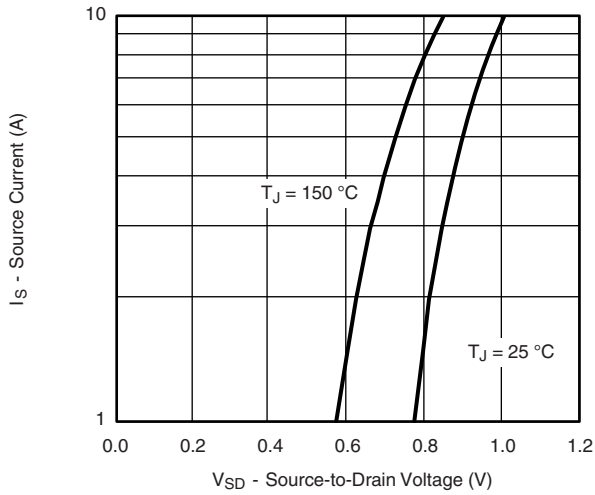


Q_g - Total Gate Charge (nC)
Gate Charge

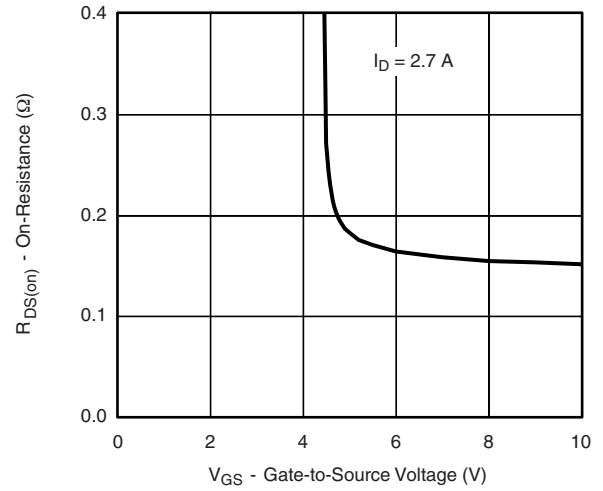


T_J - Junction Temperature ($^{\circ}\text{C}$)
On-Resistance vs. Junction Temperature

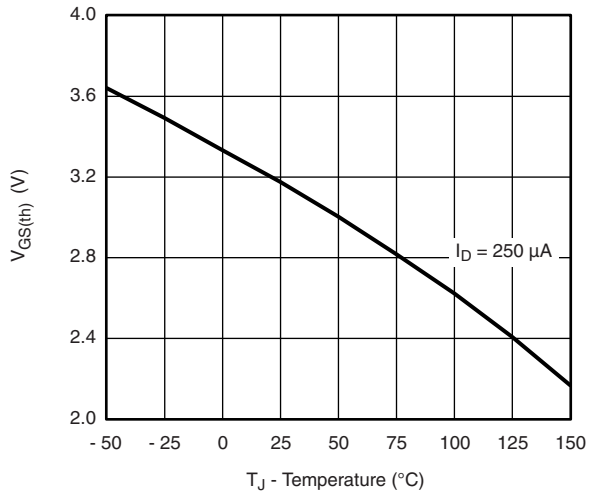
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



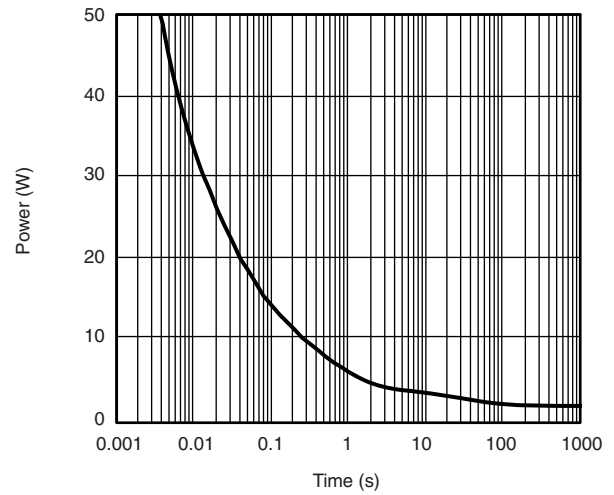
Source-Drain Diode Forward Voltage



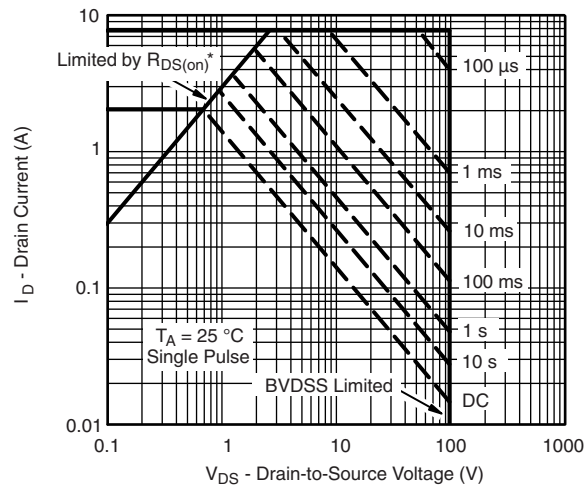
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



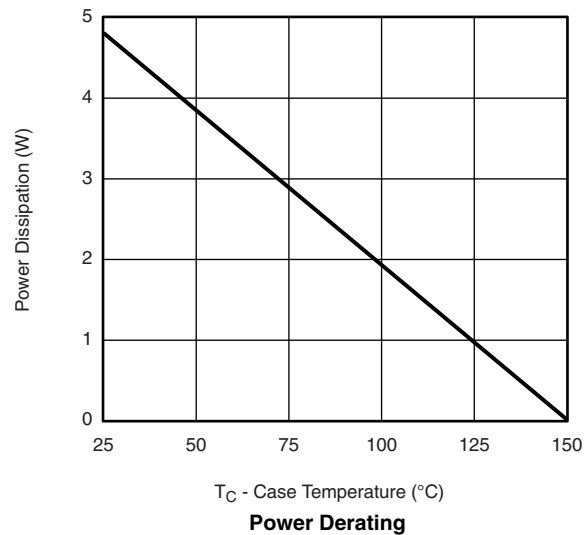
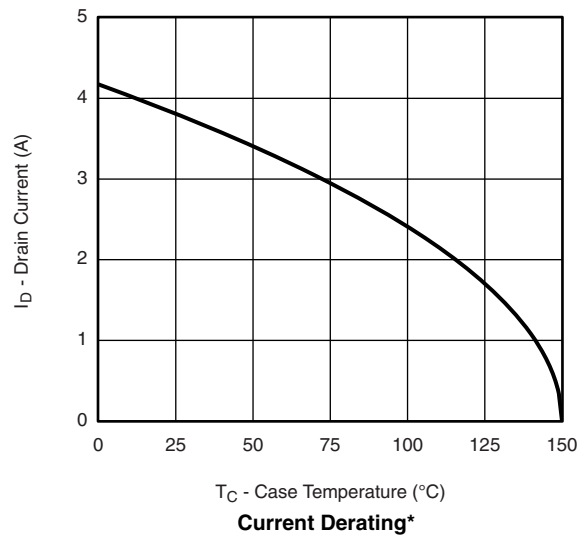
Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

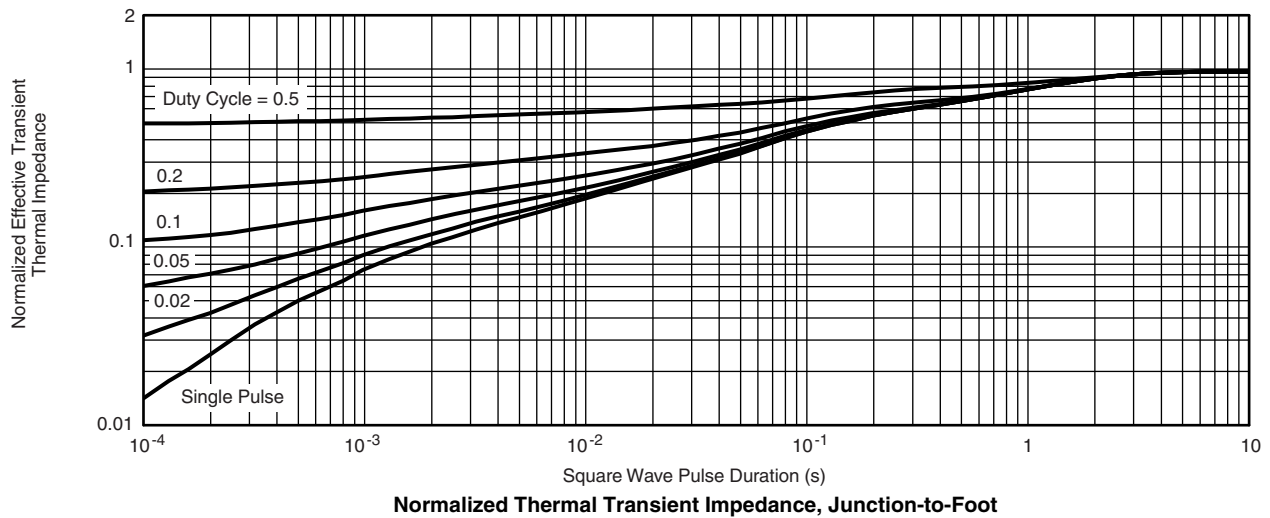
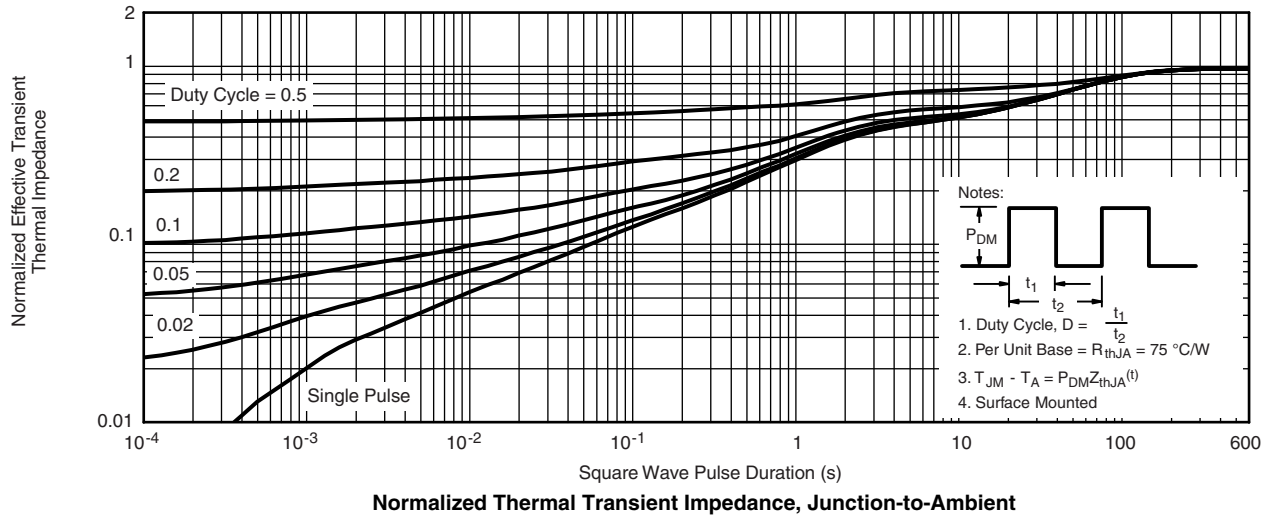
Safe Operating Area, Junction-to-Ambient

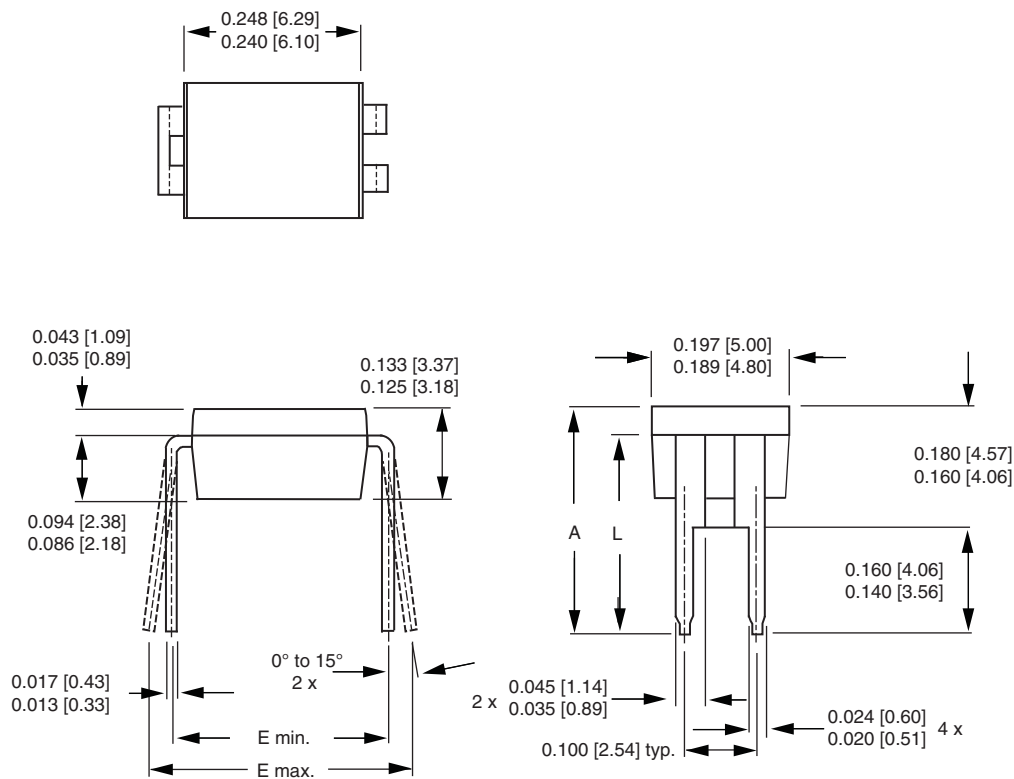
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



* The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



HVM DIP (High voltage)

DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36
ECN: X10-0386-Rev. B, 06-Sep-10 DWG: 5974				

Note

1. Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.

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