

IRFD9014PBF-VB Datasheet

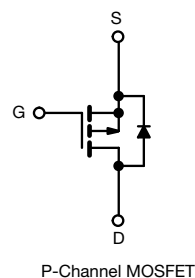
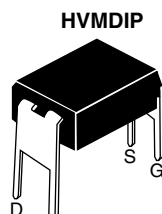
Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	-60	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10\text{ V}$	0.10
Q_g max. (nC)	19	
Q_{gs} (nC)	5.4	
Q_{gd} (nC)	11	
Configuration	Single	

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- For automatic insertion
- End stackable
- P-channel
- 175 °C operating temperature
- Fast switching


RoHS
 COMPLIANT
ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	-60	V
Gate-Source Voltage			V _{GS}	± 20	
Continuous Drain Current	V _{GS} at -10 V	T _A = 25 °C	I _D	-3.0	A
		T _A = 100 °C		-2.1	
Pulsed Drain Current ^a			I _{DM}	-15	
Linear Derating Factor				0.0083	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	180	mJ
Repetitive Avalanche Current ^a			I _{AR}	-3.0	A
Repetitive Avalanche Energy ^a			E _{AR}	0.23	mJ
Maximum Power Dissipation	T _A = 25 °C		P _D	2.3	W
Peak Diode Recovery dV/dt ^c			dV/dt	-4.5	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +175	°C
Soldering Recommendations (Peak temperature) ^d	For 10 s			300	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. $V_{DD} = -25\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 15\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = -3.2\text{ A}$ (see fig. 12).

c. $I_{SD} \leq -11\text{ A}$, $dI/dt \leq -140\text{ A/ms}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^{\circ}\text{C}$.

d. 1.6 mm from case.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$		-60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = -1\text{ mA}$		-	- 0.056	-	V/ $^\circ\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -1\text{ }\mu\text{A}$		-2.0	-	-4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	- 100	μA
		$V_{DS} = -48\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$		-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -0.96\text{ A}^b$	-	0.10	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = -25\text{ V}$, $I_D = -0.96\text{ A}^b$		1.3	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = -25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5		-	570	-	pF
Output Capacitance	C_{oss}			-	360	-	
Reverse Transfer Capacitance	C_{rss}			-	65	-	
Total Gate Charge	Q_g	$V_{GS} = -10\text{ V}$	$I_D = -11\text{ A}$, $V_{DS} = -48\text{ V}$, see fig. 6 and 13 ^b	-	-	19	nC
Gate-Source Charge	Q_{gs}			-	-	5.4	
Gate-Drain Charge	Q_{gd}			-	-	11	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30\text{ V}$, $I_D = -11\text{ A}$, $R_g = 18\text{ }\Omega$, $R_D = 2.5\text{ }\Omega$, see fig. 10 ^b		-	13	-	ns
Rise Time	t_r			-	68	-	
Turn-Off Delay Time	$t_{d(off)}$			-	15	-	
Fall Time	t_f			-	29	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L_S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 1.6	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	- 13	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = -1.6\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	-	- 6.3	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = -11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}^b$		-	100	200	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.32	0.64	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

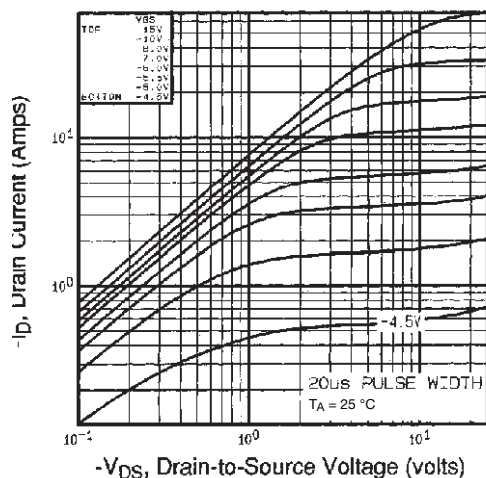


Fig. 1 - Typical Output Characteristics, $T_A = 25^\circ\text{C}$

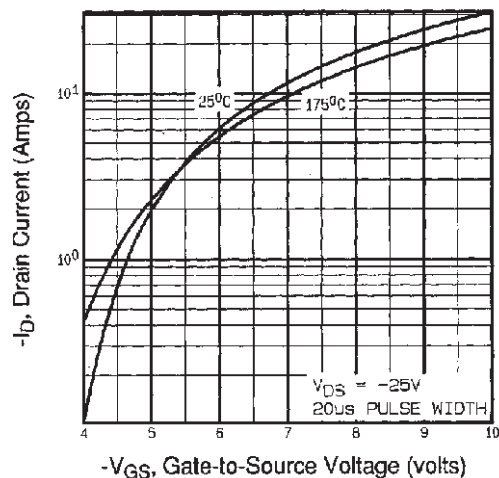


Fig. 3 - Typical Transfer Characteristics

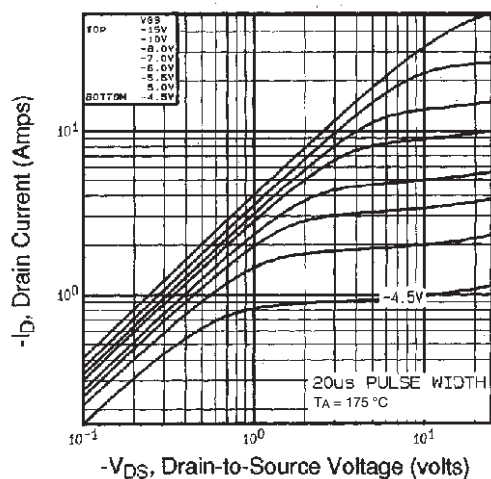


Fig. 2 - Typical Output Characteristics, $T_A = 175^\circ\text{C}$

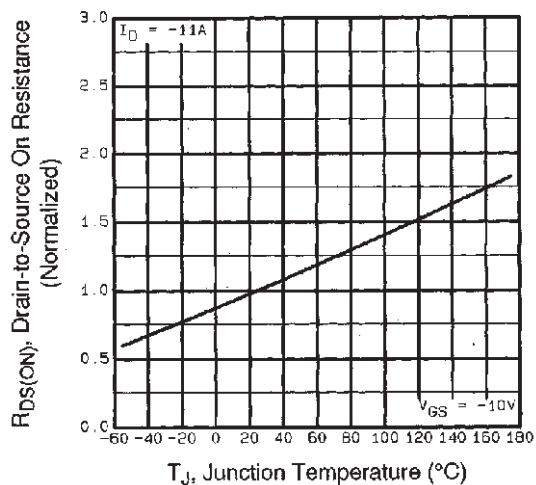


Fig. 4 - Normalized On-Resistance vs. Temperature

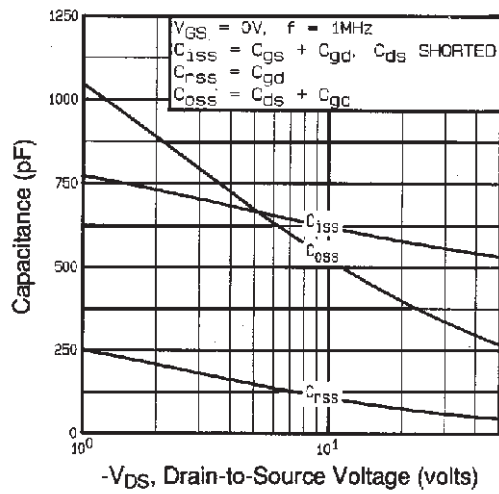


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

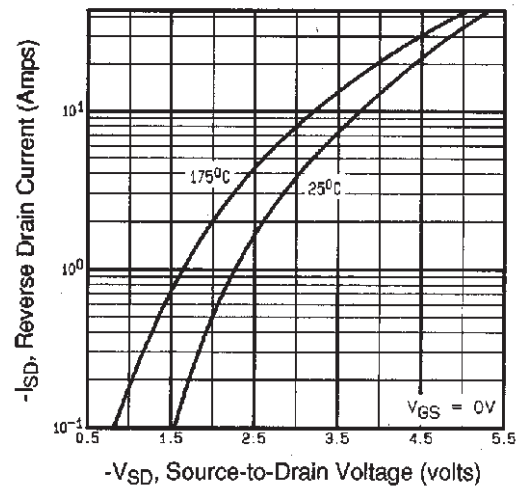


Fig. 7 - Typical Source-Drain Diode Forward Voltage

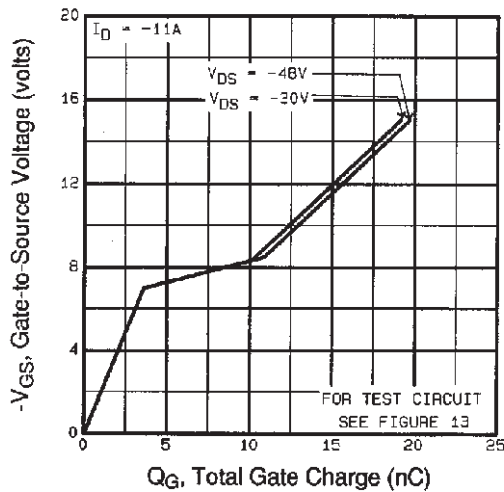


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

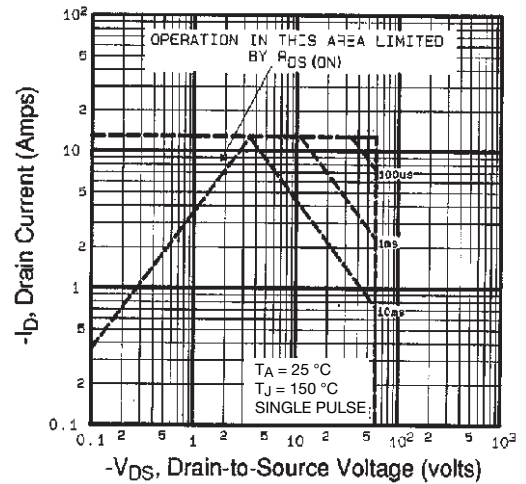


Fig. 8 - Maximum Safe Operating Area

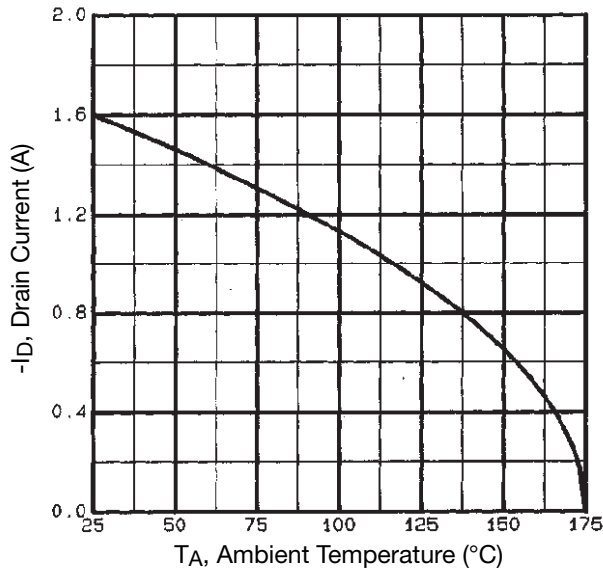


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

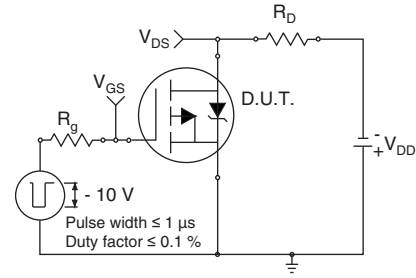


Fig. 10a - Switching Time Test Circuit

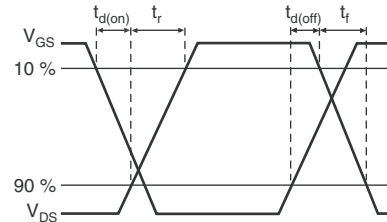


Fig. 10b - Switching Time Waveforms

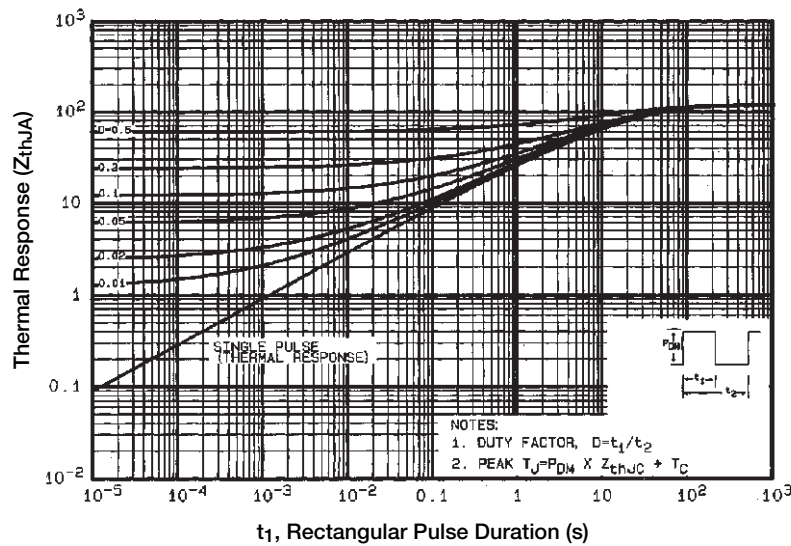


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

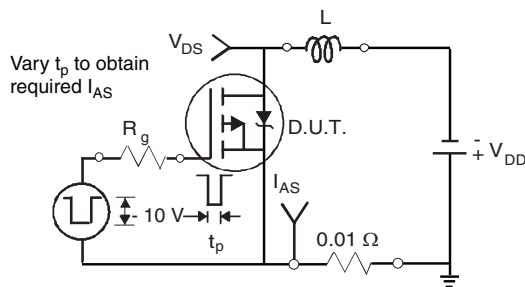


Fig. 12a - Unclamped Inductive Test Circuit

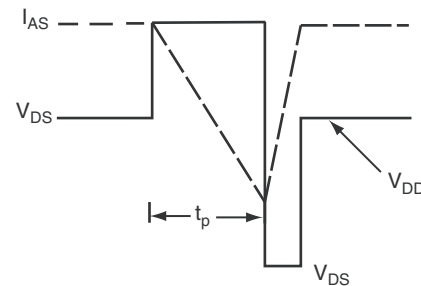


Fig. 12b - Unclamped Inductive Waveforms

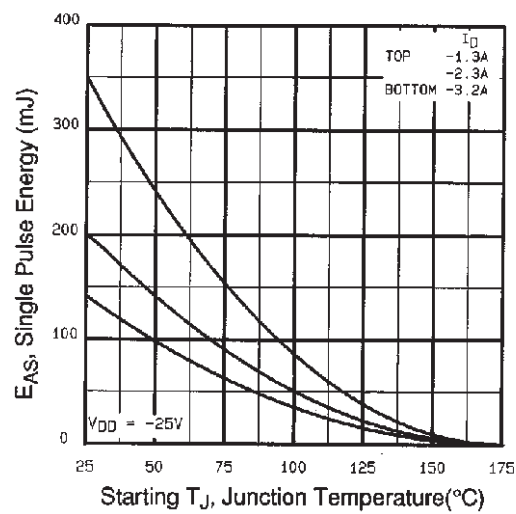


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

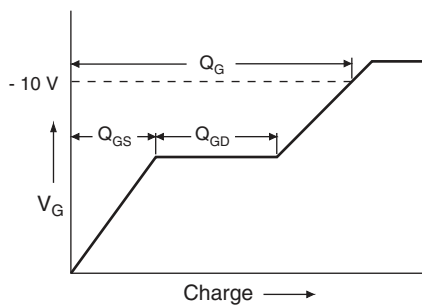


Fig. 13a - Basic Gate Charge Waveform

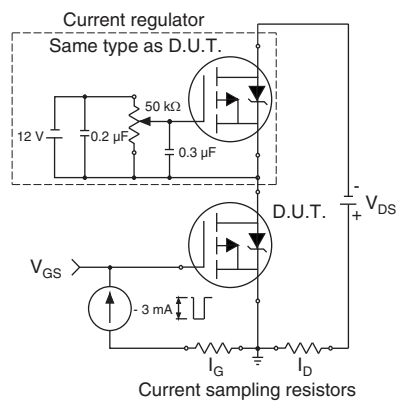
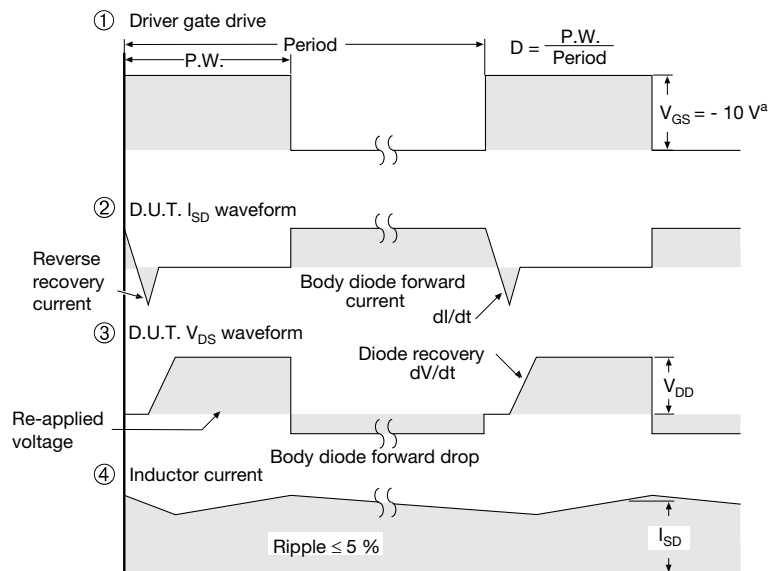
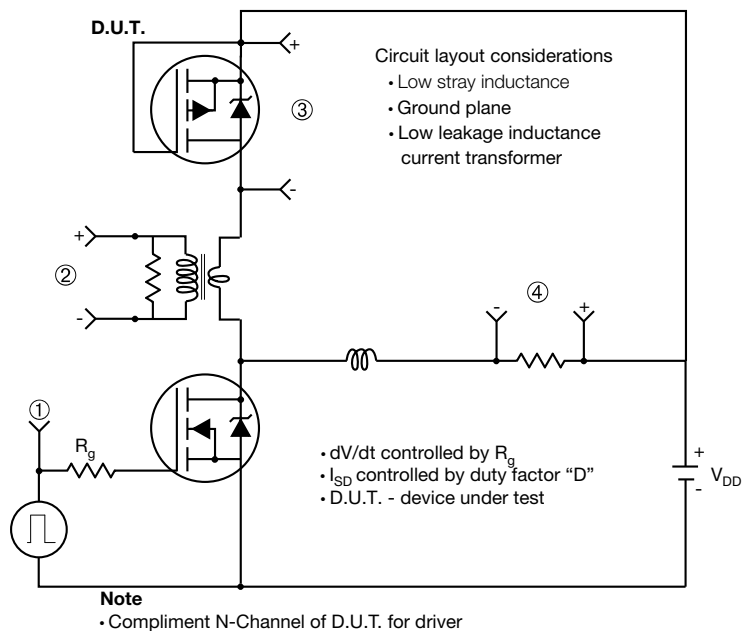


Fig. 13b - Gate Charge Test Circuit

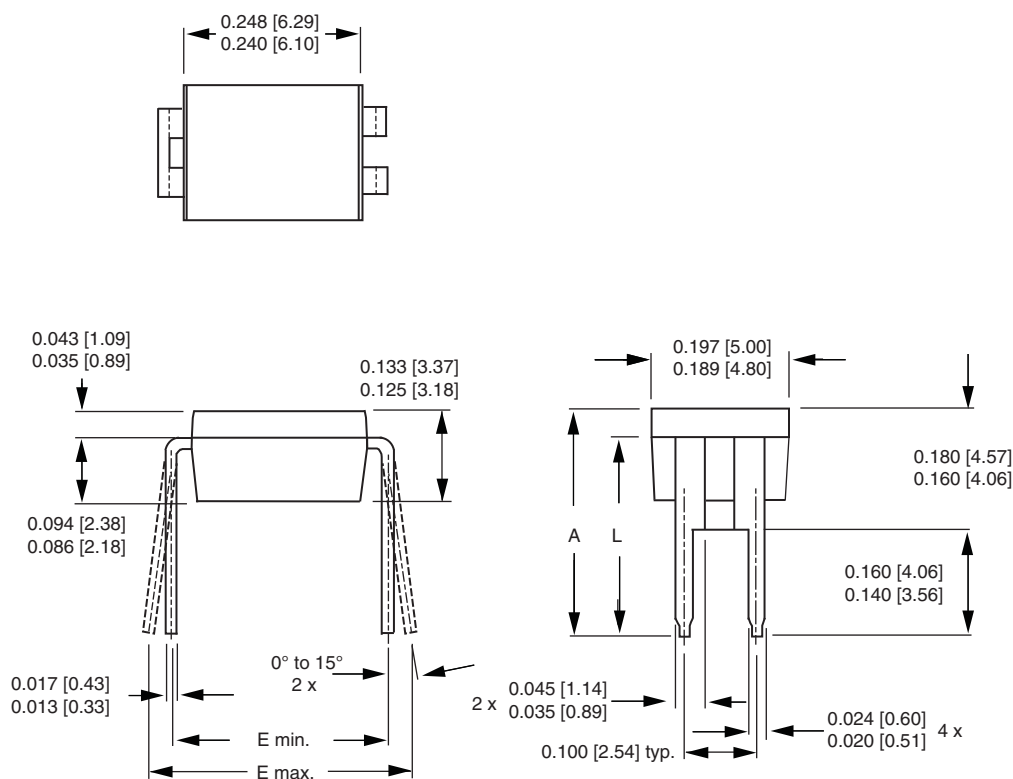
Peak Diode Recovery dV/dt Test Circuit



Note
 a. $V_{GS} = -5 V$ for logic level and $-3 V$ drive devices

Fig. 14 - For P-Channel

HVM DIP (High voltage)



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

ECN: X10-0386-Rev. B, 06-Sep-10
DWG: 5974

Note

- Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.

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