

SSP7460N-VB Datasheet

N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	60
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.024
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.028
Q_g typ. (nC)	5.2
I_D (A)	15 ^{a, g}
Configuration	Single

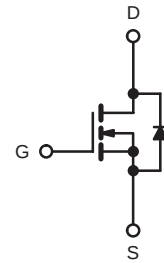
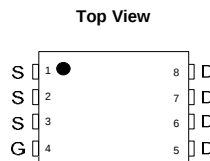
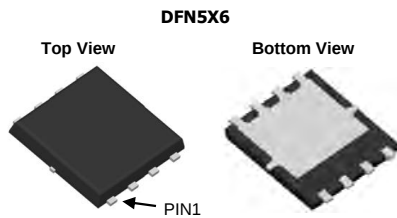
FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- Trench Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested


RoHS
 COMPLIANT

APPLICATIONS

- Battery Switch
- DC/DC Converter



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	I_D	15 ^a	A
		9 ^a	
		10.3 ^{b, c}	
		8.1 ^{b, c}	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	40	
Continuous source-drain diode current	I_S	12 ^a	
		3 ^{b, c}	
Single pulse avalanche current	I_{AS}	15	
Single pulse avalanche energy	E_{AS}	11.3	mJ
Maximum power dissipation	P_D	35.7	W
		22.9	
		3.6 ^{b, c}	
		2.3 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R_{thJA}	25	35	°C/W
Maximum junction-to-case (drain)	R_{thJC}	2.7	3.5	

Notes

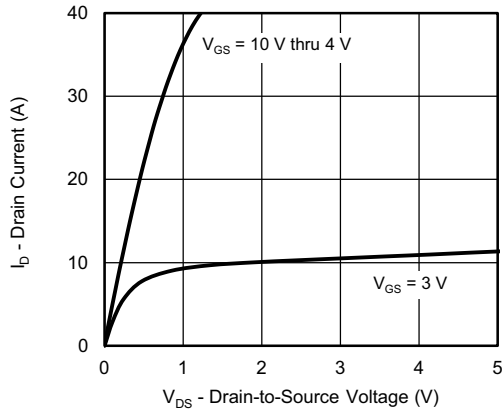
- a. Package limited
 b. Surface mounted on 1" x 1" FR4 board
 c. $t = 10$ s

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	60	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	33	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J		-	-4.8	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1	-	2.8	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 70 °C	-	-	10	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	10	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A	-	0.024	-	Ω
		V _{GS} = 4.5 V, I _D = 5 A	-	0.028	-	
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 10 A	-	39	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz	-	790	-	pF
Output capacitance	C _{oss}		-	330	-	
Reverse transfer capacitance	C _{rss}		-	14	-	
Total gate charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 5 A	-	11.1	17	nC
Gate-source charge	Q _{gs}	V _{DS} = 30 V, V _{GS} = 4.5 V, I _D = 5 A	-	5.2	8	
Gate-drain charge	Q _{gd}		-	2.2	-	
Gate resistance	R _g		-	1.1	-	
Turn-on delay time	t _{d(on)}	f = 1 MHz	0.1	0.6	1.2	Ω
Rise time	t _r	V _{DD} = 30 V, R _L = 6 Ω, I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	-	7	15	ns
Turn-off delay time	t _{d(off)}		-	21	40	
Fall time	t _f		-	10	20	
Turn-on delay time	t _{d(on)}		-	10	20	
Rise time	t _r	V _{DD} = 30 V, R _L = 6 Ω, I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	13	25	
Turn-off delay time	t _{d(off)}		-	25	50	
Fall time	t _f		-	10	20	
Fall time	t _f		-	22	45	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	15	-	A
Pulse diode forward current	I _{SM}		-	-	40	
Body diode voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.79	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 5 A, di/dt = 100 A/μs, T _J = 25 °C	-	30	60	ns
Body diode reverse recovery charge	Q _{rr}		-	60	120	nC
Reverse recovery fall time	t _a		-	15	-	ns
Reverse recovery rise time	t _b		-	15	-	

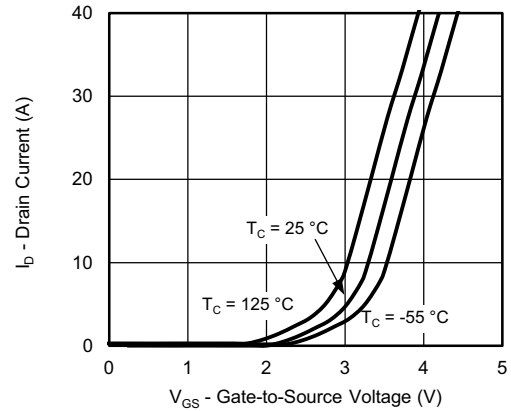
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
 b. Guaranteed by design, not subject to production testing

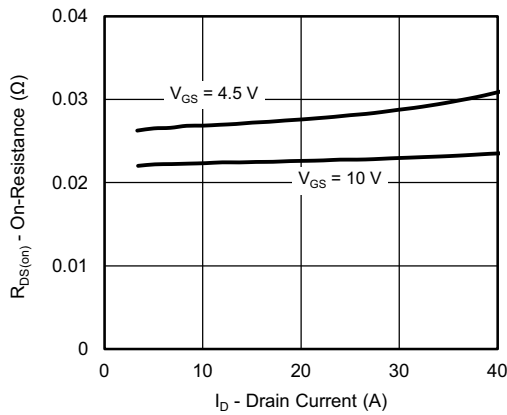
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



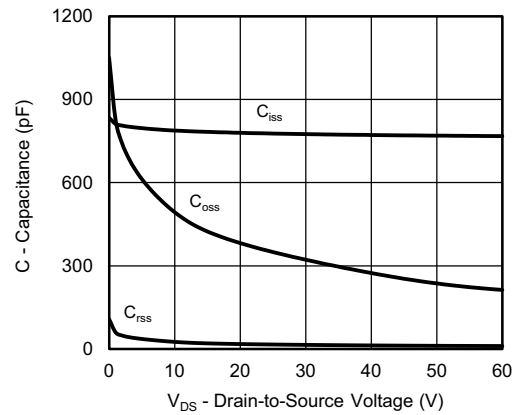
Output Characteristics



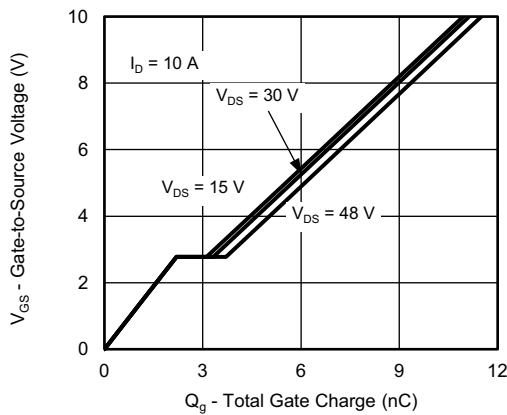
Transfer Characteristics



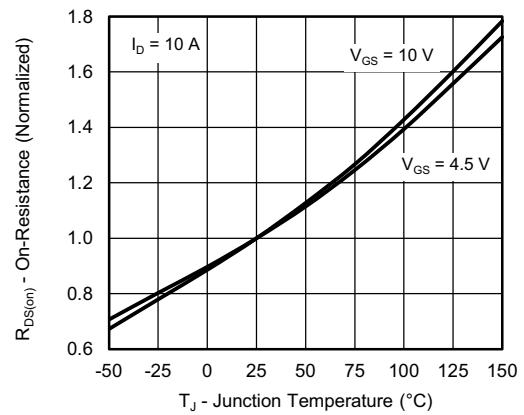
On-Resistance vs. Drain Current and Gate Voltage



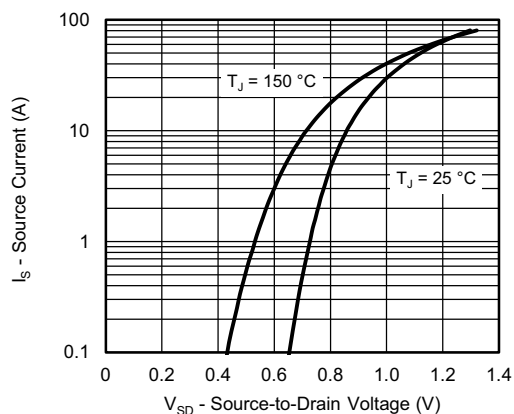
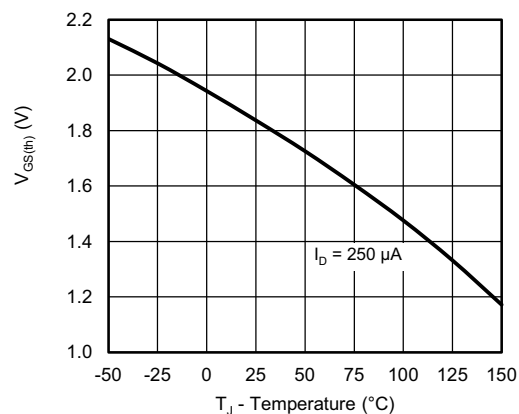
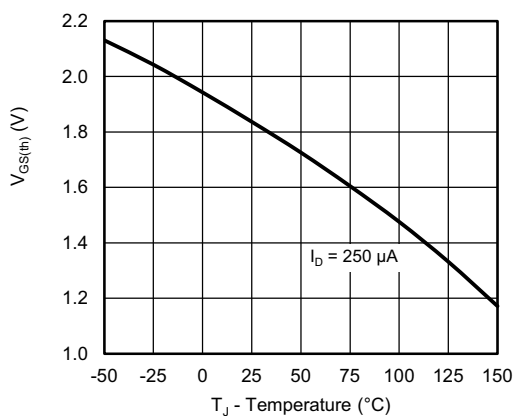
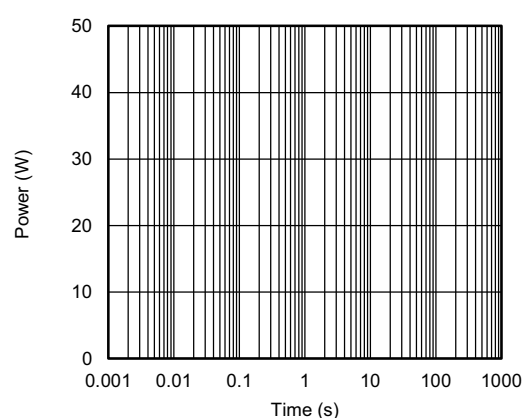
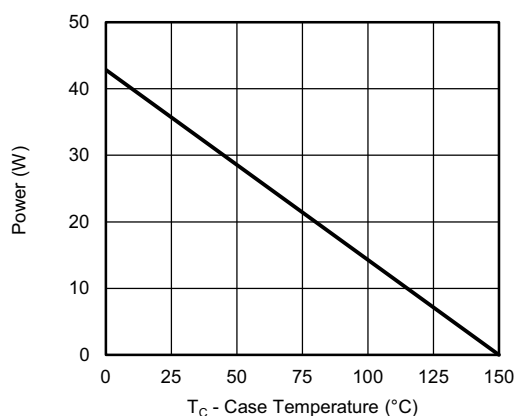
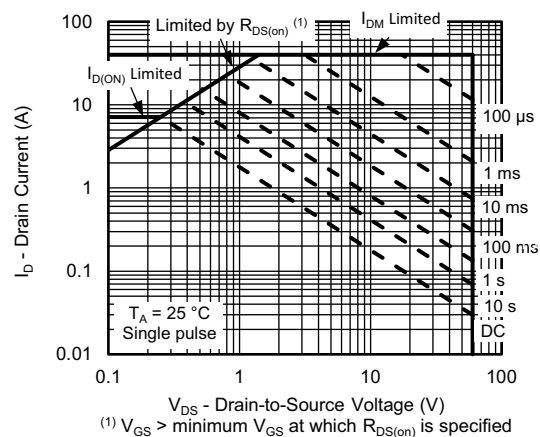
Capacitance

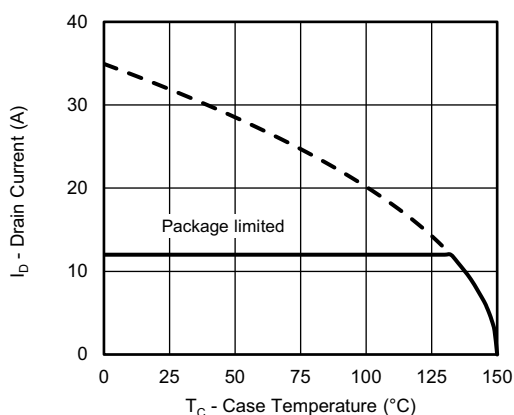


Gate Charge

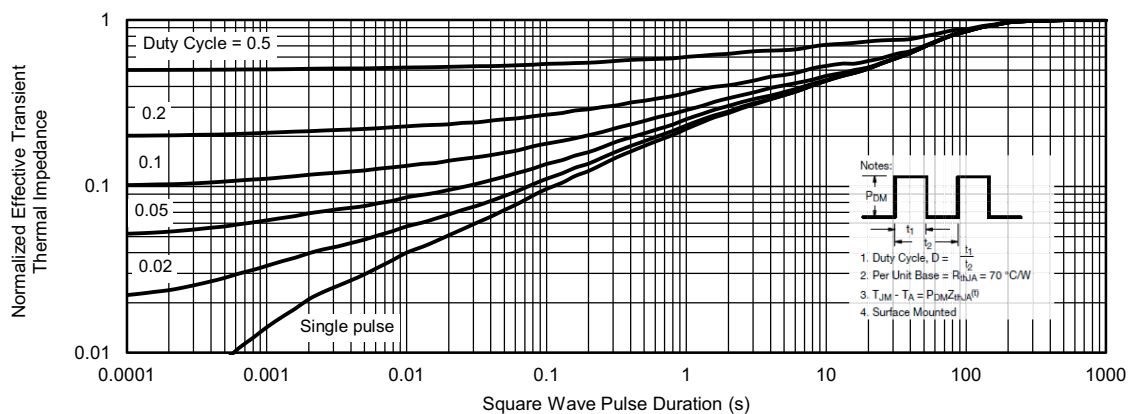
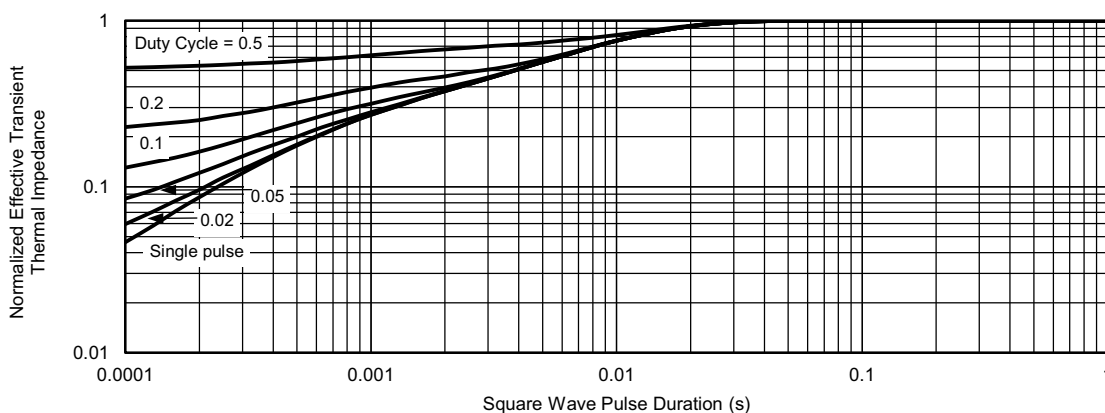


On-Resistance vs. Junction Temperature

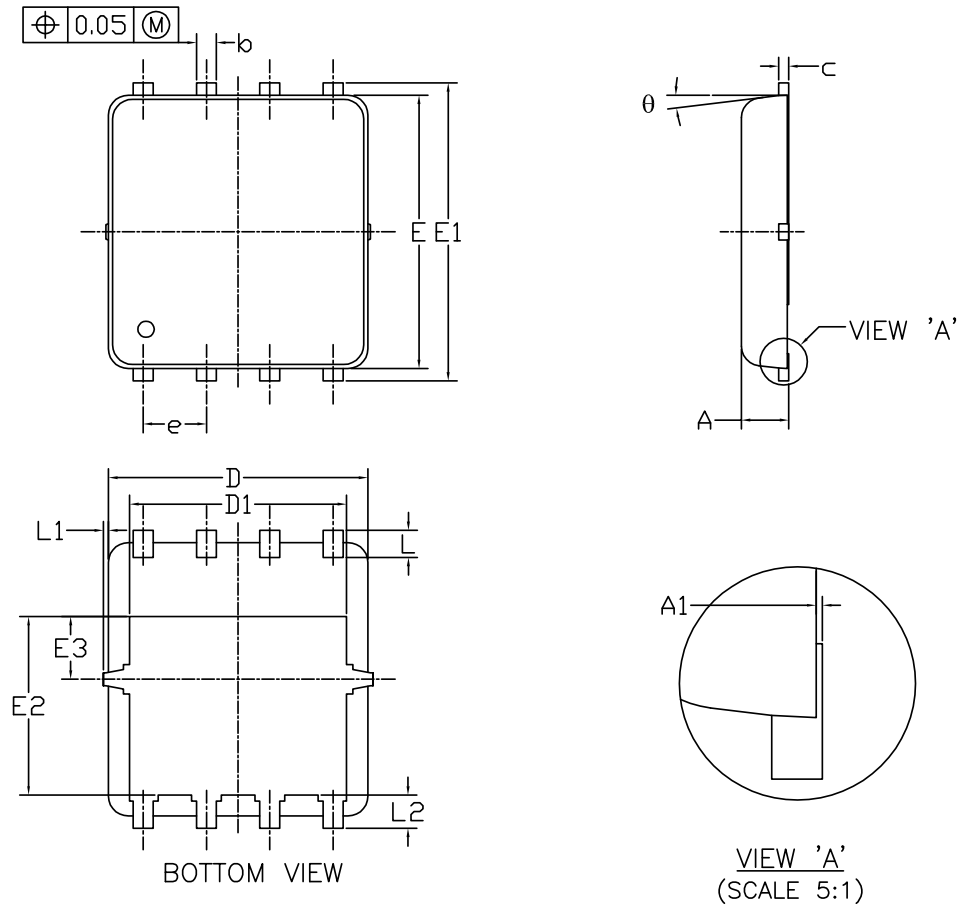
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**Source-Drain Diode Forward Voltage****Threshold Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient****Power, Junction-to-Case****Safe Operating Area, Junction-to-Ambient**

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a
Note

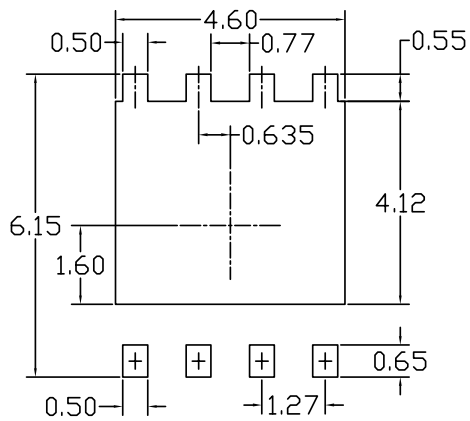
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit


Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Foot

DFN5x6_8L_EP1_P PACKAGE OUTLIN



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	---	0.05	0.000	---	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.10	5.20	5.30	0.201	0.205	0.209
D1	4.25	4.35	4.45	0.167	0.171	0.175
E	5.45	5.55	5.65	0.215	0.219	0.222
E1	5.95	6.05	6.15	0.234	0.238	0.242
E2	3.525	3.625	3.725	0.139	0.143	0.147
E3	1.175	1.275	1.375	0.046	0.050	0.054
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	---	0.15	0	---	0.006
L2	0.68 REF			0.027 REF		
θ	0°	---	10°	0°	---	10°

NOTE

UNIT: mm

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
2. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT

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