

### **Power MOSFET**

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	850				
$R_{DS(on)}(\Omega)$	V <sub>GS</sub> = 10 V 6.5				
Q <sub>g</sub> (Max.) (nC)	38				
Q <sub>gs</sub> (nC)	5.0				
Q <sub>gd</sub> (nC)	21				
Configuration	Single				

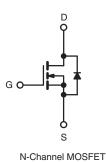
#### **FEATURES**

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC









PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V <sub>DS</sub>	850	V	
Gate-Source Voltage			V <sub>GS</sub>	± 20	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C T <sub>C</sub> = 100 °C	,	2.0		
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 100 °C	I <sub>D</sub>	1.4	Α	
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	7.2				
Linear Derating Factor				0.43	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	180	mJ	
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	2.0	Α	
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	5.4	mJ	
Maximum Power Dissipation $T_C = 25  ^{\circ}C$			P <sub>D</sub>	54	W	
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	2.0	V/ns	
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature) for 10 s				300 <sup>d</sup>	7 0	
Maunting Tayous	6 00 or M			10	lbf ⋅ in	
Mounting Torque	6-32 or M3 screw			1.1	N⋅m	

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b.  $V_{DD}$  = 50 V, starting  $T_J$  = 25 °C, L = 104 mH,  $R_g$  = 25  $\Omega$ ,  $I_{AS}$  = 1.8 A (see fig. 12). c.  $I_{SD}$  ≤ 1.8 A, dI/dt ≤ 80 A/µs,  $V_{DD}$  ≤ 600,  $T_J$  ≤ 150 °C.

- d. 1.6 mm from case.



THERMAL RESISTANCE RATINGS						
PARAMETER	UNIT					
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	62			
Case-to-Sink, Flat, Greased Surface	R <sub>thCS</sub>	0.50	-	°C/W		
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	2.3			

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static					l		
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		850		-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference t	to 25 °C, I <sub>D</sub> = 1 mA	-	0.98	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V$	<sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>G</sub>	<sub>S</sub> = ± 20 V	-	-	± 100	nA
7. 0.1 1/1 1/1 1/1 1/1 1/1 1/1 1/1 1/1 1/1 1	_	V <sub>DS</sub> = 85	V <sub>DS</sub> = 850 V, V <sub>GS</sub> = 0 V		-	100	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 680 V, V	/ <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	500	μA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 1.1 A <sup>b</sup>	-	6.5	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 10	00 V, I <sub>D</sub> = 1.1 A <sup>b</sup>	0.80	-	-	S
Dynamic					ı		
Input Capacitance	C <sub>iss</sub>	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ f = 1.0  MHz,  see fig. 5		-	530	-	pF
Output Capacitance	C <sub>oss</sub>			-	150	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	90	-	
Total Gate Charge	Qg			-	-	38	nC
Gate-Source Charge	$Q_{gs}$	V <sub>GS</sub> = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 1.8 \text{ A}, V_{DS} = 425 \text{ V},$ see fig. 6 and 13 <sup>b</sup>		-	5.0	
Gate-Drain Charge	Q <sub>gd</sub>	1			-	21	
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DD} = 425 \text{V, I}_D = 1.8 \text{ A,}$ $R_g = 18 \ \Omega, \ R_D = 230 \ \Omega, \ \text{see fig. } 10^b$		-	8.2	-	ns
Rise Time	t <sub>r</sub>			-	17	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	58	-	
Fall Time	t <sub>f</sub>			-	27	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	
Internal Source Inductance	L <sub>S</sub>			-	7.5	-	- nH
<b>Drain-Source Body Diode Characteristic</b>	s						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		ı	-	1.8	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	7.2	7
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub>	<sub>S</sub> = 1.8 A, V <sub>GS</sub> = 0 V <sup>b</sup>	-	-	1.4	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T 05 °C 1	1 0 A Al/At 400 A/b	-	380	570	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	$T_J = 25  ^{\circ}\text{C}, I_F = 1.8  \text{A}, dI/dt = 100  \text{A}/\mu\text{s}^b$		-	0.94	1.4	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-	rn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )			L <sub>D</sub> )	

#### Notes

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- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. Pulse width  $\leq$  300 µs; duty cycle  $\leq$  2 %.



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

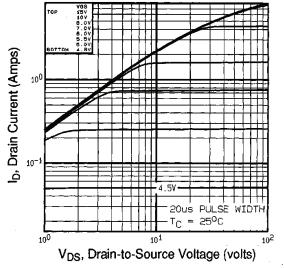
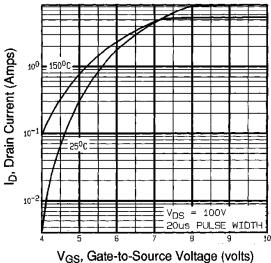


Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C



V<sub>GS</sub>, Gate-to-Source Voltage (Volts) Fig. 3 - Typical Transfer Characteristics

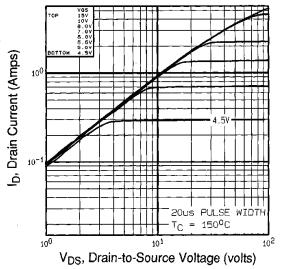


Fig. 2 - Typical Output Characteristics,  $T_C$  = 150 °C

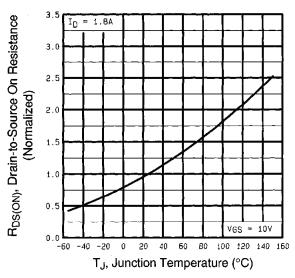


Fig. 4 - Normalized On-Resistance vs. Temperature

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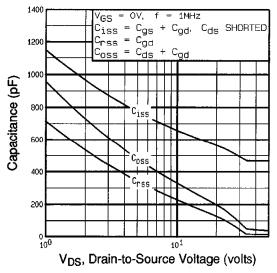


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

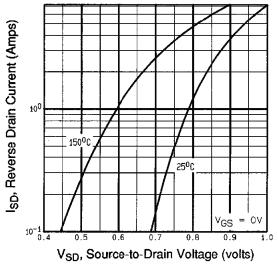


Fig. 7 - Typical Source-Drain Diode Forward Voltage

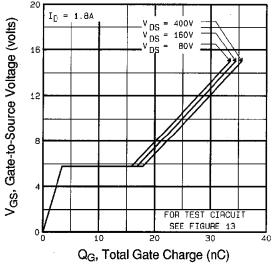


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

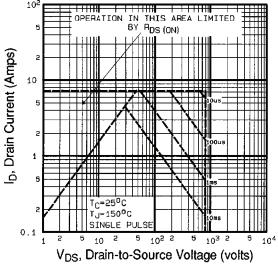


Fig. 8 - Maximum Safe Operating Area



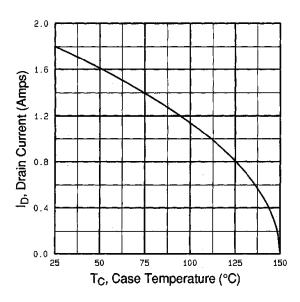


Fig. 9 - Maximum Drain Current vs. Case Temperature

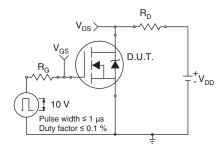


Fig. 10a - Switching Time Test Circuit

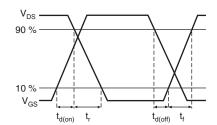


Fig. 10b - Switching Time Waveforms

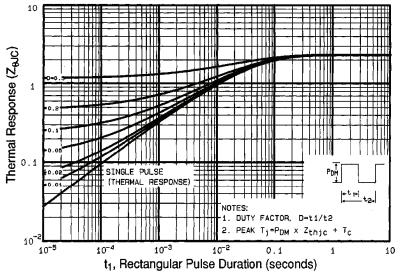
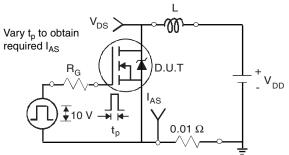
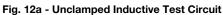


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case







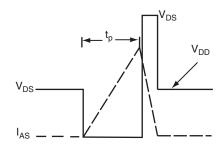


Fig. 12b - Unclamped Inductive Waveforms

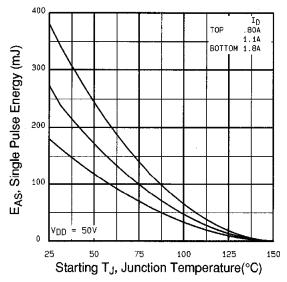


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

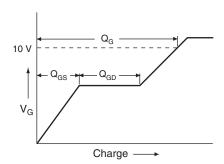


Fig. 13a - Basic Gate Charge Waveform

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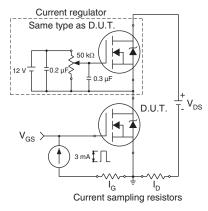
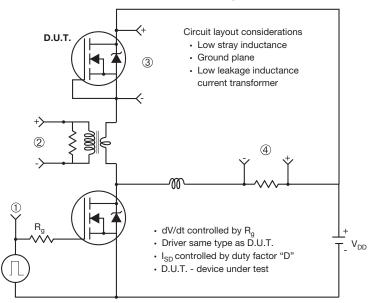


Fig. 13b - Gate Charge Test Circuit



#### Peak Diode Recovery dV/dt Test Circuit



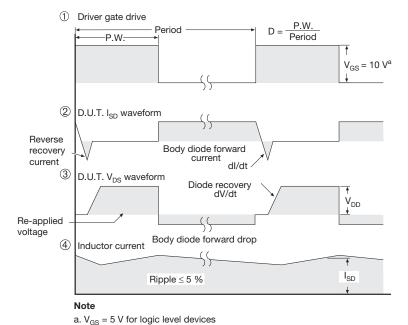
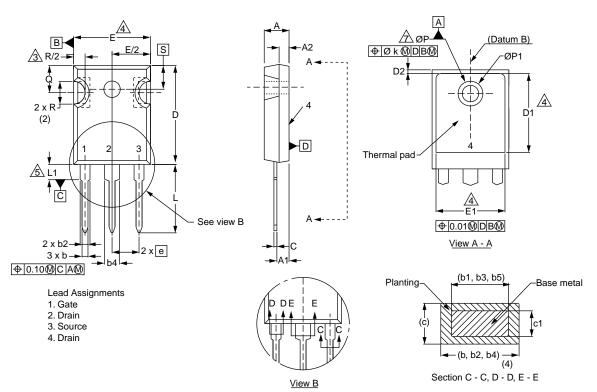


Fig. 14 - For N-Channel



# **TO-247AC (High Voltage)**



	MILLIMETERS		INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
Α	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
С	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

	MILLIM	IETERS	INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
е	5.46	BSC	0.215 BSC	
Øk	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
ØΡ	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217	BSC



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